REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

The Examiner rejects Claims 1-5, 10, 11, 16 and 17 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states that Claim 1 is misdescriptive and rendered the claim indefinite because the error amplifier recited in Line 5 is separated from the main current loop. The Examiner states that as shown in the drawing, the error amplifier is part of the main current loop.

This rejection and the Examiner's statement that the error amplifier is part of the main current loop is respectfully traversed. Referring to FIGURE 3, there is an error amplifier 16, which is not part of the main current loop. This is clearly stated in Paragraph **[023]** at Lines 4-5 which recites an LDO loop 10 and a current limit loop 12. Loop 10 is shown in FIGURE 3 in the dashed lines and loop 12 is separately demarcated. Therefore, the Examiner's objection is incorrect and should be withdrawn. Claim 1 has been amended in order to recite a main current loop error amplifier and sensing loop error amplifier, in order to clarify this for the Examiner.

The Examiner states that claims 3, 10 and 16 are indefinite because it is unclear as what impedance level is considered low. The Examiner states in claims 4, 11 and 17 are indefinite because it is unclear as what impedance level is considered high. These claims have been amended by citing that the error amplifier has first and second or a plurality of output nodes, and the output is connected to either the lower or higher impedance node. The Examiner rejects claims 2-5 as including the indefiniteness of Claim 1. This indefiniteness having been traversed above, these claims are allowable for the same reason.

The Examiner rejects claims 1-5 under 35 U.S.C. § 102(e) as being anticipated by Kadanka. The Examiner states that Kadanka discloses in FIGURE 2 a method of stabilizing two current loops within a circuit comprising the steps of providing a main current loop which the Examiner states is loop comprising elements 12, 50, R1, R2, and 40 and for supplying a

current to a load and providing a sensing loop which the Examiner states is the loop comprising elements 22, 16, 14, and error amplifier 12 coupled to the output of the sensing loop such that the capacitance of each loop is isolated from that of the other loop and providing capacitance, which the Examiner states are elements 40 and 14, to each loop whereby stability is independently maintained for each loop within the selected operating criteria.

This rejection is respectfully traversed. First of all, the loop comprising elements 22, 50, and 14 does contain a compensation capacitor 14, but the load capacitance 40 is not a compensation capacitor. This is clearly because a load capacitance can change with the load and is not available to the designer of the LDO regulator to compensate the main loop. Referring to Column 4, Lines 22-26, the reference states that both the load resistance and the load capacitance may vary. Accordingly, if the capacitor 40 were utilized to compensate the main loop, it would only be compensated during certain portions of normal operation.

More importantly, while Kadanka does show a main loop, the second loop described by the Examiner is not a current monitoring loop for controlling the current to the load, it is a zero generating loop which provides a load-dependent zero in order to compensate the main loop for stability. See, for example, Column 5, Lines 33-40. It should also be noted that the "second loop", as defined by the Examiner, does not contain an error amplifier as recited in Claim 1. Claim 1 has been amended by reciting that the sensing loop controls the current to the load, which is clearly distinguished from Kadanka.

The Examiner rejects Claims 1-18 under 35 U.S.C. § 103(a) as being unpatentable over Kadanka in view of Chen. The Examiner states that FIGURE 2 of Kadanka shows all of the limitations of the claim except for the detail of the differential amplifier. The Examiner states that Chen's FIGURE 1 shows a differential amplifier having the advantage of lower power consumption and concludes that it would have been obvious to one of ordinary skill in the art to use Chen's amplifier for Kadanka's amplifier for the purpose of improving the circuit.

We can not agree. First of all, the Examiner's argument must fail for the same reasons given above with respect to Kadanka. It is noted that Kadanka only provides a single loop, the second "loop" recited by the Examiner being a variable zero source. Thus, assuming arguendo, that Kadanka were combined with Chen, the differential amplifier of Chen would be substituted for the transistor in Kadanka, and would result in a moveable zero which uses a differential amplifier. It would not result in a separate sensing loop for control in a current to a load, as recited in Claim 1. Furthermore, Chen's circuit of FIGURE 2 is an operational amplifier which has a cascade stage between the input stage and the output stage. There is nothing in this reference, either singly or when combined with Kadanka, that shows or suggests that two (2) loops can be provided in the same circuit where the compensating capacitance of each loop independently maintains stability for the loops.

Accordingly, Applicants believe the Application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
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